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FOR

A METHOD FOR ETCHING A THIN METAL LAYER

Inventors:

Justin K. Brask
Mark L. Doczy
Jack Kavalieros
Uday Shah
Matthew V. Metz
Robert S. Chau
Robert B. Turkot, Jr.

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Teresa Edwards
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A METHOD FOR ETCHING A THIN METAL LAYER

FIELD OF THE INVENTION

[0001] The present invention relates to methods for etching metal layers, in particular, those formed when making semiconductor devices.

BACKGROUND OF THE INVENTION

[0002] It may be desirable to use a metal gate electrode when making a MOS field-effect transistor that includes a high-k gate dielectric. When forming such a metal gate electrode, it may be necessary to remove portions of a previously deposited very thin metal layer. As shown in figure 1a, patterned masking layer 102 may define sections of metal layer 101 to be removed. If a wet etch process is applied to remove part of metal layer 101, that process may etch metal layer 101 isotropically. As a consequence, part of metal layer 101 may be etched from beneath masking layer 102, as figure 1b illustrates. The resulting undercut may have adverse consequences.

[0003] Accordingly, there is a need for an improved process for etching a very thin metal layer. There is a need for such a process that may enable part of such a layer to be removed, without removing significant portions of it from beneath an overlying masking layer. The method of the present invention provides such a process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figures 1a-1b illustrate a process for etching a metal layer.

[0005] Figures 2a-2b represent cross-sections of structures that may be formed when carrying out an embodiment of the method of the present invention.

[0006] Figures 3a-3c identify hexa-dentate chelating agents that may be used in an embodiment of the method of the present invention.

[0007] Figures 4a-4c represent cross-sections of structures that may be formed when carrying out a second embodiment of the method of the present invention.

[0008] Figures 5a-5g represent cross-sections of structures that may be formed when carrying out a third embodiment of the method of the present invention.

[0009] Features shown in these figures are not intended to be drawn to scale.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0010] A method for etching a metal layer is described. That method comprises forming a metal layer on a substrate, then exposing part of the metal layer to a wet etch chemistry that comprises an active ingredient with a diameter that exceeds the thickness of the metal layer. In the following description, a number of details are set forth to provide a thorough understanding of the present invention. It will be apparent to those skilled in the art, however, that the invention may be practiced in many ways other than those expressly described here. The invention is thus not limited by the specific details disclosed below.

[0011] Figures 2a-2b illustrate structures that may be formed, when carrying out an embodiment of the method of the present invention. Initially, metal layer 201 is formed on substrate 200. Masking layer 202 is then deposited and patterned to generate the figure 2a structure. Metal layer 201 preferably is less than about 100 angstroms thick, and more preferably is between about 25 angstroms and about 50 angstroms thick. Metal layer 201 may comprise any metal that may be etched. Examples of such metals include: hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel, metal carbides and conductive metal oxides. Metal layer 201 may be formed on substrate 200 using a conventional PVD or CVD process, as will be apparent to those skilled in the art. Masking layer 202 preferably comprises a silicon nitride or silicon dioxide hard mask, which may be deposited and patterned in the conventional manner.

[0012] After masking layer 202 is patterned, exposed part 203 of metal layer 201 is removed, generating the figure 2b structure. In the method of the present invention, exposed part 203 of metal layer 201 is removed using a wet etch chemistry that comprises

an active ingredient. That active ingredient preferably comprises an etchant that is associated with a sufficient number of water molecules to solubilize the etchant. The resulting complex -- which may have a quasi-spherical configuration and may be identified as a "hydrated etchant" -- must have a diameter that exceeds the thickness of metal layer 201.

[0013] In a particularly preferred embodiment, a wet etch chemistry comprising an aqueous solution that includes a chelating agent (e.g., an organic compound that may bind to a metal ion to form a chelate) is applied to exposed part 203 of metal layer 201 to remove that part of that layer. Examples of potentially useful chelating agents include those that have been employed to remove metallic contaminants from semiconductor substrates. Particularly preferred are hexa-dentate chelating agents (i.e., chelating agents with six bonding atoms). Figures 3a-3c identify some hexa-dentate chelating agents that may be used, including carboxylic acid based chelating agents 301 and 302 (EDTA and CDTA, respectively); catechol 303 (representative of phenol derivatives that may be used); and phosphonic acid based chelating agents 304 and 305 (c-TRAMP and DTPMP). When such well known chelating agents are added to an aqueous solution to etch metal layer 201, they should be included at a concentration of between about 0.5 and about 5.0 moles/liter.

[0014] In contrast to the method that figures 1a-1b illustrate, the method described above ensures that significant amounts of metal layer 201 will not be removed from beneath masking layer 202, when exposed part 203 of metal layer 201 is removed. In a preferred embodiment, less than about 100 angstroms of metal layer 201 are removed from beneath masking layer 202, when exposed part 203 of metal layer 201 is removed. In a more preferred embodiment, less than about 50 angstroms of metal layer 201 are removed from beneath masking layer 202, when exposed part 203 of metal layer 201 is removed.

[0015] Figures 4a-4c illustrate a process for making a semiconductor device that employs the method of the present invention. Initially, high-k gate dielectric layer 401 is formed on substrate 400, and metal layer 402 is formed on high-k gate dielectric layer 401. Part of metal layer 402 is then masked by masking layer 403 -- generating the figure 4a structure.

[0016] Substrate 400 may comprise any material upon which a semiconductor device may be built. High-k gate dielectric layer 401 may comprise, for example, hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, or lead zinc niobate. Particularly preferred are hafnium oxide, zirconium oxide, and aluminum oxide. Metal layer 402 may comprise any conductive material from which a metal gate electrode may be derived. In this regard, metal layer 402 may comprise one of the materials identified above in connection with metal layer 201.

[0017] High-k gate dielectric layer 401 and metal layer 402 may be formed on substrate 400 using conventional PVD and CVD deposition methods. A conventional atomic layer CVD process preferably is used to deposit high-k gate dielectric layer 401. High-k gate dielectric layer 401 preferably is between about 5 angstroms and about 40 angstroms thick. Metal layer 402 preferably is less than about 100 angstroms thick, and more preferably is between about 25 angstroms and about 50 angstroms thick. Masking layer 403 may comprise a polysilicon layer, which may be deposited and patterned using conventional deposition, photolithography and etch techniques.

[0018] A wet etch chemistry that comprises an aqueous solution that contains a chelating agent may be applied to exposed part 404 of metal layer 402 to remove that part of that layer, and to generate the figure 4b structure. As in the embodiment described above, hexa-dentate chelating agents may be used to etch metal layer 402. Removing exposed

portion 404 of metal layer 402 using a wet etch chemistry that includes such a chelating agent may enable metal layer 402 to be etched selectively to high-k gate dielectric layer 401, without significantly etching that metal layer from beneath masking layer 403. After metal layer 402 is etched, the exposed portion of high-k gate dielectric layer 401 may be removed using any etch process suitable for removing such a layer, yielding the figure 4c structure.

[0019] Figures 5a-5g illustrate a process for making a CMOS semiconductor device that employs the method of the present invention. Figure 5a represents a cross-section of a structure that includes: high-k gate dielectric layer 501, which is formed on substrate 500; first metal layer 502, which is formed on high-k gate dielectric layer 501; and masking layer 503, which is formed on first metal layer 502.

[0020] High-k gate dielectric layer 501 may comprise one of the materials identified above. In one embodiment, first metal layer 502 comprises an n-type metal, for example: hafnium, zirconium, titanium, tantalum, aluminum, and metal carbides that include these elements. First metal layer 502 may be formed on high-k gate dielectric layer 501 using a well known PVD or CVD process, and preferably is between about 25 angstroms and about 50 angstroms thick. When first metal layer 502 comprises an n-type material, that layer preferably has a workfunction that is between about 3.9 eV and about 4.2 eV.

[0021] Dopants may be added to first metal layer 502, as it is formed or after it is formed, to shift layer 502's workfunction to ensure that it falls within the desired range. The optimal concentration of any dopant that is added to first metal layer 502 to shift its workfunction to a targeted level may depend upon the composition and properties of layer 502 (including its initial workfunction), the type of dopant used, and the target workfunction. Metal layers that are doped as, or after, they are deposited fall within the definition of "metal layer," as that term is used in this application.

[0022] Masking layer 503 may be formed from conventional materials, e.g., silicon nitride or silicon dioxide, using conventional techniques. After masking layer 503 is deposited on layer 502, conventional photolithography and etch processes may be applied to remove part of masking layer 503, exposing a first portion of first metal layer 502 and yielding the figure 5a structure.

[0023] After patterning masking layer 503, a first portion of first metal layer 502 is removed, leaving part of high-k gate dielectric layer 501 exposed. A plasma dry etch process, e.g., one using a chlorine based plasma, may be applied to remove a first portion of layer 502 selective to high-k gate dielectric layer 501. Although a dry etch process is preferred, a wet etch process may be used instead as long as it does not remove a significant amount of layer 502 from beneath masking layer 503. After first metal layer 502 is etched, the remainder of masking layer 503 is removed, generating the figure 5b structure.

[0024] In this embodiment, second metal layer 504 is then deposited on first metal layer 502 and on the exposed portion of high-k gate dielectric layer 501 – generating the structure illustrated by figure 5c. When first metal layer 502 comprises an n-type metal, second metal layer 504 preferably comprises a p-type metal. Examples of potentially suitable p-type metals for forming second metal layer 504 include: ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide.

[0025] Second metal layer 504 may be formed on high-k gate dielectric layer 501 and first metal layer 502 using a conventional PVD or CVD process, and preferably is between about 25 angstroms and about 50 angstroms thick. When second metal layer 504 comprises a p-type material, layer 504 preferably has a workfunction that is between about 4.9 eV and about 5.2 eV.

[0026] As with first metal layer 502, dopants may be added to second metal layer 504 to shift layer 504's workfunction to the desired level. In some embodiments, first metal layer

502 and second metal layer 504 may each comprise the same mid-gap metal, e.g., titanium nitride or tantalum nitride. The workfunction of a layer that includes such a mid-gap metal may be shifted up or down by adding an element to that layer that has a relatively low electronegativity or a relatively high electronegativity. When an n-type metal is desired for first metal layer 502, the workfunction of that layer may be shifted to about 4.2 eV or less by adding to a mid-gap metal an element with a relatively low electronegativity, e.g., aluminum. When a p-type metal is desired for second metal layer 504, the workfunction of that layer may be shifted to about 4.9 eV or higher by adding to a mid-gap metal an element with a relatively high electronegativity, e.g., chlorine.

[0027] Although a few examples of materials that may be used to form first and second metal layers 502 and 504 are described here, those layers may be made from many other materials. The term "metal layer," as applied in this embodiment, thus encompasses any conductive material from which a metal gate electrode may be derived.

[0028] After depositing second metal layer 504 on first metal layer 502 and high-k gate dielectric layer 501, masking layer 505 is deposited on second metal layer 504. Masking layer 506 is then formed on masking layer 505 and patterned to define sections of masking layer 505 to be removed and sections to be retained. Figure 5d represents a cross-section of the structure that results after masking layer 506 is deposited on masking layer 505, and then patterned.

[0029] In a preferred embodiment, masking layer 505 comprises a polysilicon containing layer, which may be deposited using conventional methods and which preferably is between about 500 angstroms and about 2,000 angstroms thick. Such a polysilicon layer may be undoped or doped with either n-type or p-type impurities. Layer 506 may comprise conventional materials, e.g., silicon nitride or silicon dioxide, and may be deposited and patterned using conventional techniques.

[0030] After layer 506 is patterned, a first portion of layer 505 is removed selective to second metal layer 504 to expose part of layer 504 and to create the figure 5e structure. A dry etch process may be used to etch layer 505. Such a dry etch process may employ a plasma that is derived from sulfur hexafluoride, hydrogen bromide, hydrogen iodide, chlorine, argon, oxygen and/or helium. The optimal process for etching layer 505 may depend upon the material used for second metal layer 504, the degree to which layer 505 is doped, and the desired profile for the resulting etched layer.

[0031] The exposed portion of second metal layer 504 and the underlying portion of first metal layer 502 are then removed, to generate the figure 5f structure. To prevent that process step from removing significant portions of layers 504 and 502 from beneath masking layer 505, layers 504 and 502 are removed with a wet etch process that employs a chelating agent, like those identified above. When such well known chelating agents are added to an aqueous solution to etch metal layers 504 and 502, they should be included at a concentration of between about 0.5 and about 5.0 moles/liter.

[0032] Depending upon the materials used for metal layers 504 and 502 and for high-k gate dielectric layer 501, it may be desirable to modify the chelating agents described above (or to employ other types of chelating agents) to ensure that layers 504 and 502 are etched selectively to layer 501. A chelating agent that is tailored to bind with ions of a specific metal may selectively etch a layer that includes that metal without significantly etching an underlying film having a different composition. In this respect, parts of a chelating agent, e.g., aryl or alkyl groups, may be modified to enhance its ability to bind to a specific metal (or metals) to enable selective etching of that metal.

[0033] When second metal layer 504 and first metal layer 502 comprise multiple components, a wet etch chemistry for etching those layers may include multiple chelating agents -- with different agents having an affinity to bind to different components that are

contained in those layers. The relative concentration of each chelating agent included in such a solution may be proportional to the relative amounts of each component included in the metal layers.

[0034] The chelating agent or agents selected for the wet etch chemistry used to etch layers 504 and 502 should be combined with a suitable solvent to maximize etch selectively. The best solvent for etching layers 504 and 502 selectively to layer 501 may be de-ionized water. In other embodiments, the optimum solvent may be acidic or basic, and may comprise many types of polar and/or nonpolar components, depending upon the composition of layers 504, 502, and 501. Although in a preferred embodiment, the same wet etch chemistry is used to etch both layers 504 and 502, different wet etch chemistries may be used to etch those layers.

[0035] When the combination of layers 504 and 502 is less than about 100 angstroms thick, exposing those layers to a wet etch chemistry that includes a chelating agent or agents may etch those layers selectively to high-k gate dielectric layer 501, without significantly etching those materials from beneath masking layer 505. In a preferred embodiment, using such a wet etch chemistry to etch layers 504 and 502 ensures that less than about 100 angstroms of those layers will be removed from beneath masking layer 505. In an even more preferred embodiment, such an etch process will undercut masking layer 505 by less than about 50 angstroms.

[0036] After metal layers 504 and 502 are etched, the exposed portion of high-k gate dielectric layer 501 is removed, generating the figure 5g structure. Process steps for completing the device that follow the dielectric layer etch, e.g., forming source and drain regions and the device's contacts, are well known to those skilled in the art and will not be described in more detail here. In this regard, using a dummy doped polysilicon layer for

masking layer 505 may enable one to apply commonly used nitride spacer, source/drain, and silicide formation techniques, when completing the structure.

[0037] The order in which metal layers of different conductivity type are deposited is unimportant. As illustrated, first metal layer 502 may comprise an n-type metal, and second metal layer 504 may comprise a p-type metal. Alternatively, first metal layer 502 may comprise a p-type metal, and second metal layer 504 may comprise an n-type metal.

[0038] As illustrated above, the method of the present invention enables an exposed portion of a very thin metal layer to be etched without removing significant portions of that layer where located beneath a masking layer. Although the embodiments described above provide examples of processes for carrying out this method, the present invention is not limited to these particular embodiments.

[0039] Although the foregoing description has specified certain steps and materials that may be used in the present invention, those skilled in the art will appreciate that many modifications and substitutions may be made. Accordingly, it is intended that all such modifications, alterations, substitutions and additions be considered to fall within the spirit and scope of the invention as defined by the appended claims.